ATS9870

1 GS/s 8-Bit PCI Express Digitizer

- 1.6 GB/s PCI Express (8-lane) interface
- 2 channels sampled at 8-bit resolution
- 1 GS/s simultaneous real-time sampling rate on each input
- Up to 4 GigaByte dual-port memory
- Continuous streaming mode
- ±200mV to ±4V input range
- Asynchronous DMA device driver
- AlazarDSO oscilloscope software
- Software Development Kit supports C/C++, C#, MATLAB and LabVIEW
- Linux driver available

RoHS compliant 2002/95/EC

Product	Bus	Operating System	Channels	Sampling Rate	Bandwidth	Memory Per Channel	Resolution
ATS9870	PCIe x8	Win XP/Vista/7, Linux 2.6+ 32bit/64 bit	2	1 GS/s to 1 KS/s	450 MHz	Up to 4 GB in single channel mode	8 bits

Overview

ATS9870 is an 8-lane PCI Express (PCIe x8), dual-channel, high speed, 8 bit, 1 GS/s waveform digitizer card capable of streaming acquired data to PC memory at rates up to 1.6 GB/s or storing it in its deep on-board dual-port acquisition memory buffer of up to 4 Gigabyes.

Users can capture data from one trigger or a burst of triggers. Users can also stream very large datasets continuously to PC memory or hard disk.

ATS9870 allows users to build real-time data acquisition systems even under the Windows or Linux operating systems, as users are allowed to read acquired data even while the next acquisition is in progress.

ATS9870 PCI Express digitizers are an ideal solution for cost sensitive OEM applications that require a digitizer to be embedded into the customer's equipment.

ATS9870 is supplied with AlazarDSO software that lets the user get started immediately without having to go through a software development process.

Users who need to integrate the ATS9870 in their own program can purchase a software development kit, ATS-SDK for C/C++ and MATLAB, or ATS-VI for LabVIEW for Windows or a Linux based ATS-Linux.

All of this advanced functionality is packaged in a low power, half-length PCI Express card.

PCI Express Bus Interface

ATS9870 interfaces to the host computer using an 8-lane PCI Express (Gen 1) bus. ATS9870 is also fully compatible with PCIe Gen 2 and Gen 3.

According to PCIe specification, an 8-lane board can be plugged into any 8-lane or 16-lane slot, but not into a 4-lane or 1-lane slot. As such, ATS9870 requires at least one free 8-lane or 16-lane slot on the motherboard.

The physical and logical PCIe x8 interface is provided by an on-board FPGA, which also integrates acquisition control functions, memory management functions and acquisition datapath. This very high degree of integration maximizes product reliability.

PCI Express throughput performance may vary from motherboard to motherboard. AlazarTech's 1.6 GB/s benchmark was done using ASUS P6T7 and P9X79 Pro motherboards.

Other motherboards. such as Intel S5000PSL and various Dell and HP workstations, produced similar results.

Users must always be wary of throughput specifications from manufacturers of waveform digitizers. Some unscrupulous manufacturers tend to specify the raw, burst-mode throughput of the bus.

AlazarTech, on the other hand, specifies the benchmarked sustained throughput. To achieve such high throughput, a great deal of proprietary memory management logic and kernel mode drivers have been designed.

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Analog Input
An ATS9870 features two analog input channels with extensive functionality. Each channel has 450 MHz of full power analog input bandwidth.

With software selectable attenuation, you can achieve an input voltage range of ±200mV to ±4V.

It must be noted that input impedance of both channels is fixed at 50Ω.

Software selectable AC or DC coupling further increases the signal measurement capability.

Acquisition System
ATS9870 PCI Express digitizers use a state of the art dual 1 GSPS, 8-bit ADC to digitize the input signals. The real-time sampling rate ranges from 1 GS/s down to 1 KS/s. The two channels are guaranteed to be simultaneous, as they share the exact same clock.

An acquisition can consist of multiple records, with each record being captured as a result of one trigger event. A record can contain both pre-trigger and post-trigger data.

Infinite number of triggers can be captured by ATS9870, when it is operating using dual-port memory.

In between the multiple triggers being captured, the acquisition system is re-armed by the hardware within 64 sampling clock cycles.

This mode of capture, sometimes referred to as Multiple Record, is very useful for capturing data in applications with a very rapid or unpredictable trigger rate. Examples of such applications include medical imaging, ultrasonic testing, OCT and NMR spectroscopy.

On-Board Acquisition Memory
ATS9870 supports on-board memory buffers of 256 Megabytes, 2 Gigabytes and 4 Gigabytes.

Acquisition memory can either be divided equally between the two input channels or devoted entirely to one of the channels.

There are two distinct advantages of having on-board memory:

First, a snapshot of the ADC data can be stored into this acquisition memory at full acquisition speed of 2 Gigabytes per second.

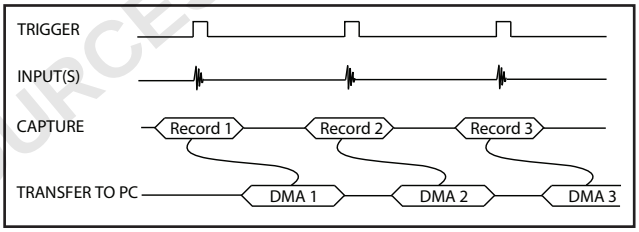
Second, and more importantly, on-board memory can also act as a very deep FIFO between the Analog to Digital converters and PCI Express bus, allowing very fast sustained data transfers across the bus, even if the operating system or another motherboard resource temporarily interrupts DMA transfers.

Maximum Sustained Transfer Rate
PCI Express support on different motherboards is not always the same, resulting in significantly different sustained data transfer rates. The reasons behind these differences are complex and varied and will not be discussed here.

ATS9870 users can quickly determine the maximum sustained transfer rate for their motherboard by inserting their card in a PCIe slot and running the Tools:Benchmark:Bus tool provided in AlazarDSO software.

ATS9870, which is equipped with dual-port on-board memory, will be able to achieve this maximum sustained transfer rate.

Traditional AutoDMA
In order to acquire both pre-trigger and post-trigger data in a dual-ported memory environment, users can use Traditional AutoDMA.



Data is returned to the user in buffers, where each buffer can contain from 1 to 8192 records (triggers). This number is called RecordsPerBuffer.

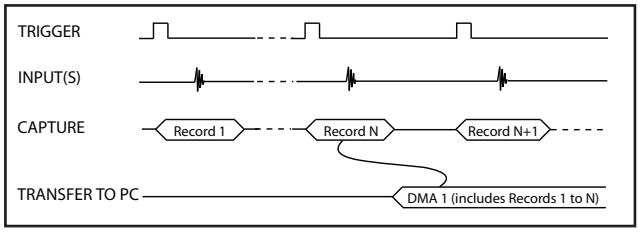
Users can also specify that each record should come with its own header that contains a 40-bit trigger timestamp.

A BUFFER_OVERFLOW flag is asserted if more than 512 buffers have been acquired by the acquisition system, but not transferred to host PC memory by the AutoDMA engine.

While Traditional AutoDMA can acquire data to PC host memory at the maximum sustained transfer rate of the motherboard, a BUFFER_OVERFLOW can occur if more than 512 triggers occur in very rapid succession, even if all the on-board memory has not been used up.

No Pre-Trigger (NPT) AutoDMA
Many ultrasonic scanning and medical imaging applications do not need any pre-trigger data: only post-trigger data is sufficient.

NPT AutoDMA is designed specifically for these applications. By only storing post-trigger data, the memory bandwidth is optimized and the entire on-board memory acts like a very deep FIFO.



Note that a DMA is not started until RecordsPerBuffer number of records (triggers) have been acquired.

NPT AutoDMA buffers do not include headers, so it is not possible to get trigger time-stamps.

More importantly, a BUFFER_OVERFLOW flag is asserted only if the entire on-board memory is used up. This provides a very substantial improvement over Traditional AutoDMA.

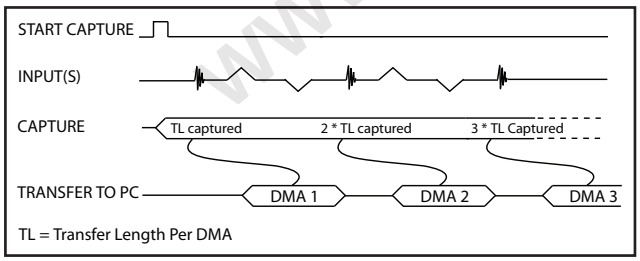
NPT AutoDMA can easily acquire data to PC host memory at the maximum sustained transfer rate of the motherboard without causing an overflow.

This is the recommended mode of operation for most ultrasonic scanning, OCT and medical imaging applications.

Continuous AutoDMA

Continuous AutoDMA is also known as the data streaming mode.

In this mode, data starts streaming across the PCI bus as soon as the ATS9870 is armed for acquisition. It is important to note that triggering is disabled in this mode.



Continuous AutoDMA buffers do not include headers, so it is not possible to get trigger time-stamps.

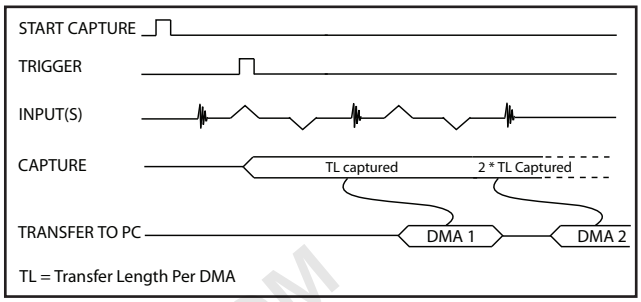
A BUFFER_OVERFLOW flag is asserted only if the entire on-board memory is used up.

The amount of data to be captured is controlled by counting the number of buffers acquired. Acquisition is stopped by an AbortCapture command.

Continuous AutoDMA can easily acquire data to PC host memory at the maximum sustained transfer rate of the motherboard without causing an overflow. This is the recommended mode for very long signal recording.

Triggered Streaming AutoDMA

Triggered Streaming AutoDMA is virtually the same as Continuous mode, except the data transfer across the bus is held off until a trigger event has been detected.



Triggered Streaming AutoDMA buffers do not include headers, so it is not possible to get trigger time-stamps.

A BUFFER_OVERFLOW flag is asserted only if the entire on-board memory is used up.

As in Continuous mode, the amount of data to be captured is controlled by counting the number of buffers acquired. Acquisition is stopped by an Abort-Capture command.

Triggered Streaming AutoDMA can easily acquire data to PC host memory at the maximum sustained transfer rate of the motherboard without causing an overflow. This is the recommended mode for RF signal recording that has to be started at a specific time, e.g. based on a GPS pulse.

Asynchronous DMA Driver

The various AutoDMA schemes discussed above provide hardware support for optimal data transfer. However, a corresponding high performance software mechanism is also required to make sure sustained data transfer can be achieved.

This proprietary software mechanism is called Async DMA (short for Asynchronous DMA).

A number of data buffers are posted by the application software. Once a data buffer is filled, i.e. a DMA has been completed, ATS9870 hardware generates an interrupt, causing an event message to be sent to the application so it can start consuming data. Once the data has been consumed, the application can post the data buffer back on the queue. This can go on indefinitely.

One of the great advantages of Async DMA is that almost 95% of CPU cycles are available for data processing, as all DMA arming is done on an event-driven basis.

To the best of our knowledge, no other supplier of waveform digitizers provides asynchronous software drivers. Their synchronous drivers force the CPU to manage data acquisition, thereby slowing down the overall data acquisition process.

Triggering

The ATS9870 is equipped with sophisticated digital triggering options, such as programmable trigger thresholds and slope on any of the input channels or the External Trigger input.

While most oscilloscopes offer only one trigger engine, ATS9870 offers two trigger engines (called Engines X and Y).

The user can specify the number of records to capture in an acquisition, the length of each record and the amount of pre-trigger data.

A programmable trigger delay can also be set by the user. This is very useful for capturing the signal of interest in a pulse-echo application, such as ultra-sound, radar, lidar etc.

Timebase

Timebase on the ATS9870 can be controlled either by on-board low-jitter VCO or by optional External Clock.

On-board low-jitter VCO uses an on-board 10 MHz TCXO as a reference clock.

Master/Slave Systems

Users can create a multi-board Master/Slave system by synchronizing up to four ATS9870 boards using an appropriate SyncBoard-9870. Note that ATS9870 board must be hardware version 1.3 or higher.

SyncBoard-9870 is available as a 2x or a 4x model: the 2x model allows a 2-board Master/Slave system whereas the 4x model allows 2, 3 or 4 board Master/Slave systems.

SyncBoard-9870 is a mezzanine board that connects to the Master/Slave connector along the top edge of the ATS9870 and sits parallel to the motherboard. For additional robustness, users can secure the SyncBoard-9870 to a bracket mounted on each of the ATS9870 boards.

The Master board's clock and trigger signals are copied by the SyncBoard-9870 and supplied to all the Slave boards. This guarantees complete synchronization between the Master board and all Slave boards.

It should be noted that SyncBoard-9870 does not use a PLL-based clock buffer, allowing the use of variable frequency clocks in Master/Slave configuration.

A Master/Slave system samples all inputs simultaneously and also triggers simultaneously on the same clock edge.

Optional External Clock

While the ATS9870 features low jitter VCO and a 10 MHz TCXO as the source of the timebase system, there may be occasions when digitizing has to be synchronized to an external clock source.

ATS9870 External Clock option provides an SMA input for an external clock signal, which can be a sine wave or LVTTL signal.

Input impedance for the External Clock input is fixed at 50 Ω. External clock input is always ac-coupled.

There are three types of External Clock supported by ATS9870. These are described below.

Fast External Clock

A new sample is taken by the on-board ADCs for each rising (or falling) edge of this External Clock signal.

In order to satisfy the clocking requirements of the ADC chips being used, Fast External Clock frequency must always be higher than 200 MHz and lower than 1 GHz.

Slow External Clock

This type of clock should be used when the clock frequency is either too slow or is a burst-type clock. Both these types of clock do not satisfy the minimum clock requirements listed above for Fast External Clock.

In this mode, the ATS9870 ADCs are run at a preset internal clock frequency. The user-supplied Slow External Clock signal is then monitored for low-to-high transitions. Each time there is such a transition, a new sample is stored into the on-board memory.

It should be noted that there can be a 0 to +8 ns sampling jitter when Slow External Clock is being used, as the internal ADC clock is not synchronized to the user-supplied clock.

Slow External Clock: $f_{EXT} < 60$ MHz

10 MHz Reference Clock

It is possible to generate the sampling clock based on an external 10 MHz reference input. This is useful for RF systems that use a common 10 MHz reference clock.

ATS9870 uses an on-board low-jitter VCO to generate the 1 GHz high frequency clock used by the ADC.

AUX Connector

ATS9870 provides an AUX (Auxiliary) BNC connector that is configured as a Trigger Output connector by default.

When configured as a Trigger Output, AUX BNC con-

nector outputs a 5 Volt TTL signal synchronous to the ATS9870 Trigger signal, allowing users to synchronize their test systems to the ATS9870 Trigger. Note that the Trigger output is synchronized to a divide-by-8 clock (dual channel mode) or divide-by-16 clock (single channel mode).

When combined with the Trigger Delay feature of the ATS9870, this option is ideal for ultrasonic and other pulse-echo imaging applications.

AUX connector can also be used as a Trigger Enable Input and Clock Output.

Real Time Signal Processing

One of the unique features of AlazarTech's waveform digitizer product line is that acquired data is available for real-time signal processing by the host CPU.

What makes this very powerful is the fact that most modern CPUs have multiple cores, which can be used to do real-time signal processing using parallel processing principles.

If your algorithm can be written to take advantage of parallel processing, this may be a very cost-effective solution for signal processing applications.

AlazarTech has been able to demonstrate that a 2.4 GHz, quad-core CPU can do real-time averaging of acquired data at 1.5 GB/s while using up only 25% of CPU cycles. A faster CPU or a CPU with more cores can do signal processing even faster.

Another very popular application is to monitor a pulse train for particle detection applications. AlazarTech has created a parallel processing algorithm that allows real time pulse detection and characterization at rates in excess of 1 GB/s.

Hardware Averaging Firmware

Many applications require hardware averaging of incoming pulses, i.e. software based averaging is not a viable option.

A custom firmware upgrade is available for ATS9870 that allows hardware averaging (co-adding) of up to 16 million records of data. Only the resulting averaged data is then transferred to computer memory as 32-bit integers.

Upgrade to this firmware disables the on-board memory, as it is not required for temporary storage of acquired data.

GPU Based Signal Processing

Graphical Processing Units (GPUs) are becoming an increasingly popular method of doing fast signal processing.

Using ATS-GPU (sold separately), ATS9870 can interface directly to an OpenCL compatible GPU using PCI Express bus. Benchmarks using a low cost Asus GTX 560 have shown that data can be acquired by ATS9870 and 4096 point FFTs can be calculated by the GPU at sustained rates up to 1 GB/s.

GPUs can also be used for many other signal processing applications.

Calibration

Every ATS9870 digitizer is factory calibrated to NIST-traceable standards. To recalibrate an ATS9870, the digitizer must either be shipped back to the factory or a qualified metrology lab.

AlazarDSO Software

ATS9870 is supplied with the powerful AlazarDSO software that allows the user to setup the acquisition hardware and capture, display and archive the signals.

An optional Stream-To-Disk add-on module for AlazarDSO allows users to stream data to hard disk. For the fastest possible streaming, the hard disks have to be used in a RAID 0 configuration.

AlazarDSO software also includes powerful tools for benchmarking the computer bus and disk drive.

Software Development Kits

AlazarTech provides easy to use software development kits for customers who want to integrate the ATS9870 into their own software.

A Windows compatible software development kit, ATS-SDK is also offered. It allows programs written in C/C++ and MATLAB to fully control the ATS9870. Sample programs are provided as source code.

A set of high performance VIs for LabVIEW 7.1 and higher, called ATS-VI, can also be purchased.

ATS-Linux

AlazarTech offers ATS9870 binary drivers for CentOS 6.3 x86_64 with kernel 2.6.32-279.5.2.el6.x86_64. These drivers are also 100% compatible with RHEL 6.3.

Also provided is a GUI application called AlazarFrontPanel that allows simple data acquisition and display.

Source code example programs are also provided, which demonstrate how to acquire data programmatically using a C compiler.

If customers want to use ATS9870 in any Linux distribution other than the one listed above, they must purchase a license for Linux driver source code and compile the driver on the target operating system. A Non-Disclosure Agreement must also be executed between the customer's organization and AlazarTech.

All such source code disclosures are made on an as-is basis with limited support from the factory.

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System Requirements

Personal computer with at least one free x8 or x16 PCI Express (v1.0a, v1.1 or v2.0) slot, 2 GB RAM, 100 MB of free hard disk space, SVGA display adaptor and monitor with at least a 1024 x 768 resolution.

Power Requirements

+12V	1.2 A, typical
+3.3V	1.1 A, typical

Physical

Size	Single slot, half length PCI card (4.2 inches x 6.5 inches)
Weight	250 g

I/O Connectors

CH A, CH B, TRIG IN, AUX I/O	BNC female connectors
ECLK	SMA female connector

Environmental

Operating temperature	0 to 55 degrees Celcius
Storage temperature	-20 to 70 degrees Celcius
Relative humidity	5 to 95%, non-condensing

Acquisition System

Resolution	8 bits
Bandwidth (-3dB)	
DC-coupled, 50Ω	DC - 450 MHz for all ranges except ±40mV range DC - 200 MHz for ±40mV range
AC-coupled, 50Ω	100KHz - 450 MHz for all ranges except ±40mV range 100 KHz - 200 MHz for ±40mV range
Bandwidth flatness:	± 1dB
Number of channels	2, simultaneously sampled
Maximum Sample Rate	1 GS/s single shot
Minimum Sample Rate	1 KS/s single shot for internal clocking
Full Scale Input ranges	
50 Ω input impedance:	±40mV, ±100mV, ±200mV, ±400mV, ±1V, ±2V, and ±4V, software selectable
DC accuracy	±2% of full scale in all ranges
Input coupling	AC or DC, software selectable
Input impedance	50Ω ±1%
Input protection	
50Ω	±4V (DC + peak AC for CH A, CH B and EXT only without external attenuation)

Amplifier Bypass Mode

Standard Feature	No
Software selectable	No. Resistor selectable. A bypass cable also must be used
Input Range	Approx. ± 256 mV
Input Coupling	DC, irrespective of the input coupling setting for the channel
Input Impedance	50 Ω, irrespective of the input impedance setting for the channel
Input bandwidth (-3dB)	450 MHz May be extended to 700 MHz as a special request

Timebase System

Timebase options	Internal Clock or External Clock (Optional)
Internal Sample Rates	1 GS/s, 500 MS/s, 250 MS/s, 100 MS/s, 50 MS/s, 20 MS/s, 10 MS/s, 5 MS/s, 2 MS/s, 1 MS/s, 500 KS/s, 200 KS/s, 100KS/s, 50 KS/s, 20 KS/s, 10 KS/s, 5 KS/s, 2 KS/s, 1 KS/s
Internal Clock accuracy	±2 ppm

Dynamic Parameters

Typical values measured on CH A of a randomly selected ATS9870. Input signal was provided by a Marconi 2018A signal generator, followed by a 9-pole, 20 MHz band-pass filter (TTE Q36T-20M-2M-50-720BMF). Input frequency was set at 20 MHz and output amplitude was 708 mV rms, which was approximately 95% of the full scale input. Input was not averaged and bandwidth limiting filter was disabled.

SNR	40.55 dB
SINAD	40.09 dB
THD	-54.8 dB
SFDR	-52.05 dB

Note that these dynamic parameters may vary from one unit to another, with input frequency and with the full scale input range selected.

Optional ECLK (External Clock) Input

Signal Level	±200mV Sine wave or 3.3V LVTTL (LVTTL for Slow External Clock only)
Input impedance	50Ω
Input coupling	AC
Maximum frequency	1 GHz for Fast External Clock 60 MHz for Slow External Clock
Minimum frequency	200 MHz for Fast External Clock DC for Slow External Clock
Sampling Edge	Rising

Optional 10 MHz Reference Input

Signal Level	±200mV sine wave
Input impedance	50Ω
Input Coupling	AC coupled

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Input Frequency	10 MHz ± 0.25 MHz
Sampling Clock Freq.	1 GHz

Triggering System

Mode	Edge triggering with hysteresis
Comparator Type	Digital comparators for internal (CH A, CHB) triggering and analog comparators for TRIG IN (External) triggering
Number of Trigger Engines	2
Trigger Engine Combination	OR, AND, XOR, selectable
Trigger Engine Source	CH A, CH B, EXT, Software or None, independently software selectable for each of the two Trigger Engines
Hysteresis	±5% of full scale input, typical
Trigger sensitivity	±10% of full scale input range. This implies that the trigger system may not trigger reliably if the input has an amplitude less than ±10% of full scale input range selected
Trigger level accuracy	±5%, typical, of full scale input range of the selected trigger source
Bandwidth	450 MHz
Trigger Delay	Software selectable from 0 to 9,999,999 sampling clock cycles
Trigger Timeout	Software selectable with a 10 us resolution. Maximum settable value is 3,600 seconds. Can also be disabled to wait indefinitely for a trigger event

TRIG IN (External Trigger) Input

Input impedance	1 KΩ in parallel with 50pF ±10pF
Bandwidth (-3dB)	
DC-coupled	DC - 450 MHz
AC-coupled	100 KHz - 450 MHz
Input range	±5V
DC accuracy	±10% of full scale input
Input protection	±8V (DC + peak AC without external attenuation)
Coupling	AC or DC, software selectable

TRIG OUT Output

Connector Used	AUX I/O
Output Signal	5 Volt TTL
Synchronization	Synchronized to a clock derived from the ADC sampling clock. Divide-by-8 clock (dual channel mode) or divide-by-16 clock (single channel mode)

Materials Supplied

ATS9870 PCI Express Card

ATS9870 Installation Disk (on USB Flash Drive)

Certification and Compliances

CE Compliance

All specifications are subject to change without notice

ORDERING INFORMATION

ATS9870-256M	ATS9870-002
ATS9870-2G	ATS9870-003
ATS9870-4G	ATS9870-004
ATS9870: External Clock Upgrade	ATS9870-005
ATS9870-FIFO to 256M Upgrade	ATS9870-007
ATS9870-FIFO to 2G Upgrade	ATS9870-008
ATS9870-FIFO to 4G Upgrade	ATS9870-009
ATS9870-256M to 2G Upgrade	ATS9870-010
ATS9870-256M to 2G Upgrade	ATS9870-011
ATS9870-256M to 4G Upgrade	ATS9870-012
ATS9870-2G to 4G Upgrade	ATS9870-013
ATS9870 Hardware Averaging Upgrade	ATS9870-014
C/C++, VB SDK for ATS9462	ATS-SDK
LabVIEW VI for ATS9870	ATS-VI
Linux Driver Source for ATS9870	ATS9870-LIN
GPU interface software for ATS9870	ATS-GPU